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COUGHLAN, PETER D	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/773,050	SALAM ET AL.	
	Examiner	Art Unit	
	Peter Coughlan	2129	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 July 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *43-48,51-67 and 70-88* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *43-48,51-67 and 70-88* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *2/5/2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Detailed Action

1. This office action is in response to an AMENDMENT entered July 25, 2007 for the patent application 10/773050 filed on February 5, 2004.

2. All previous Office Actions are fully incorporated into this Non-Final Office Action by reference.

Status of Claims

3. Claims 43-48, 51-67, 70-88 are pending.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:
A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 62-67, 70-76, 78-80 are rejected under 35 U.S.C. 102(b) (hereinafter referred to as **Oh**) being anticipated by Oh, 'Analog CMOS Implementation of Artificial Neural Networks for Temporal Signal Learning.'

Claim 62

Oh teaches an array of synaptic cells which are interconnected to form a feedforward neural network(**Oh,** p4:19 through p5:2)and configured to receive an analog input signal indicative of a biological cell measurement and to model a process of the biological cell, wherein each synaptic cell includes (**Oh,** p3:6-10; 'Configured to receive ... analog input' of applicant is disclosed by a 'subthreshold analog CMOS VLSI' of Oh.) a learning electrical circuit operable to update a local weight according to an update rule and store the local weight in a capacitor(**Oh,** p116:2-17; Oh discloses a 'master neural network' which generates weights while in the 'learning phase.' 'Learning electrical circuit' of applicant is equivalent to 'learning phase' of Oh.) a digital memory operable to store the local weight in a digital form (**Oh,** p116:2-17; Oh discloses a analog to digital converter to have analog input stored in digital form.); and a processing electrical circuit comprised of a one-dimensional multiplier which is operable to process a component of the analog input signal in accordance with the local weight stored in the digital memory. (**Oh,** abstract; 'One dimensional multiplier' of applicant is equivalent to 'vector multiplier' of Oh.)

Claim 63

Oh teaches wherein each column of synaptic cells in the array of synaptic cells represents a neuron in the neural network. (**Oh,** Figure 6.2; One function of a neuron is to use it's output for training to convergence. The column(s) of Figure 6.2 illustrate this by using the outcome of 'error' circuit for training purposes.)

Claim 64

Oh teaches an array of control cells positioned adjacent to the array of synaptic cells, where each control cell controls conversion of the local weight from an analog form to a digital form for a row of synaptic cells in the array of synaptic cells. (**Oh,** p116:2-17; Oh discloses an analog to digital converter to have analog input stored in digital form.)

Claim 65

Oh teaches wherein the control cells operate synchronously with each other to control conversion. (**Oh,** p12:14 through p13:3; Oh discloses in the McCulloch-Pitts model, in which neurons operate in asynchronous manner. Using Oh's model in which the feedforward neural network is interconnected allows synchronously operations to occur.)

Claim 66

Oh teaches wherein each control cell includes a multiplexer configured to select a synaptic cell in a given row of synaptic cells (**Oh,** figure 6.2; Figure 6.2 illustrates

numerous multiplexers within the recurrent neural network.) and an analog-to-digital converter. (**Oh,** p116:2-17)

Claim 67

Oh teaches wherein the analog-to-digital converter for a given row of synaptic cells is interconnected to each synaptic cell in the given row of synaptic cells. (**Oh,** p116:2-17)

Claim 70

Oh teaches a switch interposed between the processing circuit and the digital memory for selectively enabling use of the digital memory. (**Oh,** p116:2-17; Oh discloses a second recurrent neural network (slave neural network) which employs the weight values from the first recurrent neural network. These values are updated using the digital memory. If a user can alter between the first and second recurrent neural network, then there exists a 'switch' to do so.)

Claim 71

Oh teaches a switch interposed between the processing circuit and the learning circuit for selectively enabling use of the learning circuit. (**Oh,** p116:2-17; Oh discloses a first recurrent neural network (master neural network) which employs the learning phase of the neural network or learning circuit of applicant. These values are updated using

the digital memory. If a user can alter between the first and second recurrent neural network, then there exists a 'switch' to do so.)

Claim 72

Oh teaches a switch interposed between the processing circuit; the learning circuit and the digital memory for selectively enabling the use of either the learning circuit or the digital memory by the processing circuit. (**Oh,** p116, 2-17; If there exists two phases, a learning phase and a testing phase, then there exists a switch to alter between the two phases.)

Claim 73

Oh teaches the learning circuit is comprised of a one-dimensional multiplier for implementing the update rule. (**Oh,** abstract; 'One dimensional multiplier' of applicant is equivalent to 'vector multiplier' of Oh.)

Claim 74

Oh teaches the learning circuit is configured to receive an error signal indicative of a difference between an output signal and a target output signal. (**Oh,** p15:9 through p16:7; 'Output signal' and 'target output signal' of applicant is equivalent to 'actual output' and 'desired output' of Oh.)

Claim 73

Oh teaches multiple arrays of synaptic cells, which are interconnected to form a multi-layer neural network. (**Oh,** figure 6.2; Figure 6.2; The 2 dimensional array which each node is interconnected with other nodes of Oh is equivalent to 'multi-layer neural network' of applicant.)

Claim 76

Oh teaches the learning circuit further comprises a second multiplier configured to receive the error signal and generates a feedback propagation error signal for a previous layer in the multi-layer neural network.(**Oh,** p17:5-6 and equation (2.11); 'Error signal' of applicant is equivalent to 'w^{k}' of Oh. 'Previous layer' of applicant is equivalent to 'w^{k-1}' of Oh.)

Claim 78

Oh teaches a digital-to-analog converter interposed between the processing circuit and the digital memory in each synaptic cell. (**Oh,** p116:2-17; Oh discloses a digital to analog converter for outputting the value of the synaptic cell.)

Claim 79

Oh teaches wherein each processing circuit in a column of synaptic cells outputs a component of a weighted sum.(**Oh,** p13:4 through p15:8; 'Processing circuit in a column' of applicant is equivalent to 'the 'hidden layer' of Oh. 'Outputs a component of

a weighted sum' of applicant is equivalent to the output of each node in the hidden layer is a result of the weighted sum input.)

Claim 80

Oh teaches wherein an output of each multiplier in a column of synaptic cells is interconnected to form a weighted sum. (**Oh,** figure 5.5; Oh discloses the output of each multiplier (Y_1-Y_4) is fed back as a column to form a interconnection of synaptic cells.)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 77, 81-88 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oh as set forth above, in view of Newton. ('Newton's Telecom Dictionary', referred to as **Newton**)

Claim 77

Oh does not teach wherein the digital memory is implemented using flip-flops.

Newton teaches wherein the digital memory is implemented using flip-flops.(**Newton,** p316, C2:43-45; It is common knowledge that a flip flop circuit is used to hold digital information.) It would have been obvious to a person having ordinary skill in the art at the time of applicant's invention to modify the teachings of Oh by disclosing the flip flop circuit as taught by Newton to have the digital memory is implemented using flip-flops.

For the purpose of using industrial standard technology for containing digital values.

Claim 81

Oh teaches an array of synaptic cells which are interconnected to form a feedforward neural network(**Oh,** p4:19 through p5:2), wherein each synaptic cell includes: a learning electrical circuit operable to update a local weight according to an update rule and store the local weight in a capacitor(**Oh,** p116:2-17; Oh discloses a analog to digital converter to have analog input stored in digital form and then the digital form is used to refresh a capacitor which contains the 'weight value.'), wherein the learning circuit is comprised of a one-dimensional multiplier for implementing the update rule(**Oh,** abstract; 'One dimensional multiplier' of applicant is equivalent to 'vector multiplier' of Oh.), and is configured to receive an error signal indicative of a difference between an output signal and a target output signal (**Oh,** p15:9 through p16:7; 'Output signal' and 'target output signal' of applicant is equivalent to 'actual output' and 'desired

output' of Oh.); a digital memory operable to store the local weight in a digital form (**Oh,** p116:2-17; Oh discloses a analog to digital converter to have analog input stored in digital form.), wherein the digital memory is implemented using flip-flops (**Newton,** p316, C2:43-45; It is common knowledge that a flip flop circuit is used to hold digital information.); a processing electrical circuit comprised of a one-dimensional multiplier which is operable to process a component of an analog input signal in accordance with the local weight stored in the digital memory (**Oh,** abstract; 'One dimensional multiplier' of applicant is equivalent to 'vector multiplier' of Oh.) a switch interposed between the processing circuit, the learning circuit, and the digital memory for selectively enabling the use of either the learning circuit or the digital memory by the processing circuit(**Oh,** p116, 2-17; If there exists two phases, a learning phase and a testing phase, then there exists a switch to alter between the two phases.); a digital-to-analog converter interposed between the processing circuit and the digital memory in each synaptic cell. (**Oh,** p116:2-17)

Claim 82

Oh teaches multiple arrays of synaptic cells which are interconnected to form a multi-layer neural network (**Oh,** figure 6.2; Figure 6.2; The 2 dimensional array which each node is interconnected with other nodes of Oh is equivalent to 'multi-layer neural network' of applicant.), wherein the learning circuit further comprises a second multiplier configured to receive the error signal and generates a feedback propagation error signal for a previous layer in the multi-layer neural network. (**Oh,** p17:5-6 and equation (2.11);

'Error signal' of applicant is equivalent to 'w^k' of Oh. 'Previous layer' of applicant is equivalent to 'w^{k-1}' of Oh.)

Claim 83

Oh teaches an output of each multiplier in a column of synaptic cells is interconnected to form a weighted sum, and each processing circuit in a column of synaptic cells outputs a component of the weighted sum. (**Oh,** figure 5.5; Oh discloses the output of each multiplier (Y_1-Y_4) is a result of the summation of weights for a given row. The output of each multiplier is returned into the interconnected array as a column.)

Claim 84

Oh teaches wherein each column of synaptic cells in the array of synaptic cells represents a neuron in the neural network. (**Oh,** Figure 6.2; One function of a neuron is to use it's output for training to convergence. The column(s) of Figure 6.2 illustrate this by using the outcome of 'error' circuit for training purposes.)

Claim 85

Oh teaches an array of control cells positioned adjacent to the array of synaptic cells, where each control cell controls conversion of the local weight from an analog form to a digital form for a row of synaptic cells in the array of synaptic cells. (**Oh,**

p116:2-17; Oh discloses a analog to digital converter to have analog input stored in digital form.)

Claim 86

Oh teaches wherein the control cells operate synchronously with each other to control conversion. (**Oh,** p12:14 through p13:3; Oh discloses in the McCulloch-Pitts model, in which neurons operate in asynchronous manner. Using Oh's model in which the feedforward neural network is interconnected allows synchronously operations to occur.)

Claim 87

Oh teaches wherein each control cell includes a multiplexer configured to select a synaptic cell in a given row of synaptic cells (**Oh,** figure 6.2; Figure 6.2 illustrates numerous multiplexers within the recurrent neural network.) and an analog-to-digital converter. (**Oh,** p116:2-17)

Claim 88

Oh teaches wherein the analog-to-digital converter for a given row of synaptic cells is interconnected to each synaptic cell in the given row of synaptic cells. (**Oh,** p116:2-17)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 43-48, 51-57, 59-61 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oh as set forth above, in view of Roenker. (U. S. Patent 5509105, referred to as **Roenker**)

Claim 43

Oh teaches an array of synaptic cells, which are interconnected to form a feedforward neural network, wherein each synaptic cell includes. (**Oh,** p4:19 through p5:2)

Oh does not teach a learning electrical circuit operable to update a local weight according to an update rule and store the local weight in a capacitor in the cell.

Roenker teaches a learning electrical circuit operable to update a local weight according to an update rule and store the local weight in a capacitor in the cell.(**Roenker,** C14:48-62, C17:3-54; 'Capacitor' of applicant is equivalent to 'capacitor' of Roenker) It would have been obvious to a person having ordinary skill in the art at the

time of applicant's invention to modify the teachings of Oh by having the memory capacitor within the circuit as taught by Roenker to have a learning electrical circuit operable to update a local weight according to an update rule and store the local weight in a capacitor in the cell.

For the purpose of avoiding problem associated with a capacitor being a distance from the circuit using 'long wires'

Oh teaches a digital memory operable to store the local weight in a digital form(**Oh,** p116:2-17; Using the digital to analog converter ensures the capacitor is always refreshed, thus indicating the local weights are stored in a digital form.); and a processing electrical circuit comprised of a one-dimensional multiplier which is operable to process a component of an analog input signal in accordance with the local weight stored in the digital memory.(**Oh,** abstract; 'One dimensional multiplier' of applicant is equivalent to 'vector multiplier' of Oh.)

Claim 44

Oh teaches wherein each column of synaptic cells in the array of synaptic cells represents a neuron in the neural network. (**Oh,** Figure 6.2; One function of a neuron is to use it's output for training to convergence. The column(s) of Figure 6.2 illustrate this by using the outcome of 'error' circuit for training purposes.)

Claim 45

Oh teaches an array of control cells positioned adjacent to the array of synaptic cells, where each control cell controls conversion of the local weight from an analog form to a digital form for a row of synaptic cells in the array of synaptic cells. (**Oh,** p116:2-17; Oh discloses a analog to digital converter to have analog input stored in digital form.)

Claim 46

Oh teaches wherein the control cells operate synchronously with each other to control conversion. (**Oh,** p12:14 through p13:3; Oh discloses in the McCulloch-Pitts model, in which neurons operate in asynchronous manner. Using Oh's model in which the feedforward neural network is interconnected allows synchronously operations to occur.)

Claim 47

Oh teaches wherein each control cell includes a multiplexer configured to select a synaptic cell in a given row of synaptic cells (**Oh,** figure 6.2; Figure 6.2 illustrates numerous multiplexers within the recurrent neural network.) and an analog-to-digital converter. (**Oh,** p116:2-17)

Claim 48

Oh teaches wherein the analog-to-digital converter for a given row of synaptic cells is interconnected to each synaptic cell in the given row of synaptic cells. (**Oh,** p116:2-17)

Claim 51

Oh teaches a switch interposed between the processing circuit and the digital memory for selectively enabling use of the digital memory. (**Oh,** p116:2-17; Oh discloses a second recurrent neural network (slave neural network) which employs the weight values from the first recurrent neural network. These values are updated using the digital memory. If a user can alter between the first and second recurrent neural network, then there exists a 'switch' to do so.)

Claim 52

Oh teaches a switch interposed between the processing circuit and the learning circuit for selectively enabling use of the learning circuit. (**Oh,** p116:2-17; Oh discloses a first recurrent neural network (master neural network) which employs the learning phase of the neural network or learning circuit of applicant. These values are updated using the digital memory. If a user can alter between the first and second recurrent neural network, then there exists a 'switch' to do so.)

Claim 53

Oh teaches a switch interposed between the processing circuit, the learning circuit and the digital memory for selectively enabling the use of either the learning circuit or the digital memory by the processing circuit. (**Oh,** p116, 2-17; If there exists two phases, a learning phase and a testing phase, then there exists a switch to alter between the two phases.)

Claim 54

Oh teaches the learning circuit is comprised of a one-dimensional multiplier for implementing the update rule. (**Oh,** abstract; 'One dimensional multiplier' of applicant is equivalent to 'vector multiplier' of Oh.)

Claim 55

Oh teaches the learning circuit is configured to receive an error signal indicative of a difference between an output signal and a target output signal. (**Oh,** p15:9 through p16:7; 'Output signal' and 'target output signal' of applicant is equivalent to 'actual output' and 'desired output' of Oh.)

Claim 56

Oh teaches multiple arrays of synaptic cells, which are interconnected to form a multi-layer neural network. (**Oh,** figure 6.2; Figure 6.2; The 2 dimensional array which each node is interconnected with other nodes of Oh is equivalent to 'multi-layer neural network' of applicant.)

Claim 57

Oh teaches the learning circuit further comprises a second multiplier configured to receive the error signal and generates a feedback propagation error signal for a previous layer in the multi-layer neural network.(**Oh,** p17:5-6 and equation (2.11); 'Error signal' of applicant is equivalent to 'w^{k}' of Oh. 'Previous layer' of applicant is equivalent to 'w^{k-1}' of Oh.)

Claim 59

Oh teaches a digital-to-analog converter interposed between the processing circuit and the digital memory in each synaptic cell. (**Oh,** p116:2-17; Oh discloses a digital to analog converter for outputting the value of the synaptic cell.)

Claim 60

Oh teaches wherein each processing circuit in a column of synaptic cells outputs a component of a weighted sum.(**Oh,** p13:4 through p15:8; 'Processing circuit in a column' of applicant is equivalent to 'the 'hidden layer' of Oh. 'Outputs a component of a weighted sum' of applicant is equivalent to the output of each node in the hidden layer is a result of the weighted sum input.)

Claim 61

Oh teaches wherein an output of each multiplier in a column of synaptic cells is interconnected to form a weighted sum. (**Oh,** figure 5.5; Oh discloses the output of each multiplier (Y_1-Y_4) is fed back as a column to form a interconnection of synaptic cells.)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 58 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Oh and Roenker as set forth above, in view of Newton. ('Newton's Telecom Dictionary', referred to as **Newton**)

Claims 58, 77

Oh and Roenker do not teach wherein the digital memory is implemented using flip-flops.

Newton teaches wherein the digital memory is implemented using flip-flops.(**Newton,** p316, C2:43-45; It is common knowledge that a flip flop circuit is used to

hold digital information.) It would have been obvious to a person having ordinary skill in the art at the time of applicant's invention to modify the teachings of Oh and Roenker by disclosing the flip flop circuit as taught by Newton to have the digital memory is implemented using flip-flops.

For the purpose of using industrial standard technology for containing digital values.

Response to Arguments

5. Applicant's arguments filed on July 25, 2007 for claims 43-48, 51-67, 70-88 have been fully considered but are not persuasive.

6. In reference to the Applicant's argument:

REMARKS
Claims 43-48, 51-67 and 70-88 are now pending in the application. The Examiner is respectfully requested to reconsider and withdraw the rejections in view of the amendments and remarks contained herein.

DRAWINGS
The drawings stand objected to for certain informalities. Applicant has attached a revised drawing for the Examiner's approval. In the "Replacement Sheet", Figure 1 has been amended to define boundaries for each column that defines a neuron. The amendment is readily understood by one skilled in the art in view of the teachings of the specification as originally filed, including paragraph [0026]. Therefore, reconsideration and withdrawal of this objection is respectfully requested

Examiner's response:

The Examiner acknowledges the dotted lines which indicates the separate 'columns' or 'neurons.' The Examiner withdraws the drawing objection.

7. In reference to the Applicant's argument:

REJECTION UNDER 35 U.S.C. § 112
Claims 49, 68 and 89 stand rejected under 35 U.S.C. § 112, first paragraph, a failing to comply with the written description. This rejection is respectfully traversed. Given the teaching of the present application, one skilled in the art would readily understand how interconnects in Figure 1 could be rearranged, such that each row (as opposed to column) corresponds to a neuron. Rather than amend the specification, applicant elects to delete these claims from the application, thereby rendering the rejection moot. However, such a configuration is considered to fall within the scope of other remaining claims. Therefore, reconsideration and withdrawal of this rejection is respectfully requested

Examiner's response:

Due to the cancellation of the claims, the 35 U.S.C. §112 rejection is withdrawn.

8. In reference to the Applicant's argument:

REJECTION UNDER 35 U.S.C. § 101
Claims 43-90 stand rejected under 35 U.S.C. §101 for being nonstatutory subject matter. This rejection is respectfully traversed.

Applicant's invention is directed generally to an architecture for a chip and thus falls within one of the four statutory categories (i.e., a machine). On the contrary, the Examiner asserts that the claims are directed to an abstract concept of a chip that is/self programming. The Examiner errs by focusing only upon the preamble of the claim when formulating this rejection. The body of the pending claims clearly recite an array of cells which form a network and a particular arrangement for each cell which includes multipliers, capacitors and digital memory. These circuit components are neither an abstract idea, a law of nature, nor a natural phenomena. Therefore, the pending claims

do not fall within a judicial exception to statutory subject matter. As a result, there is no need for the pending claims to recite a practical application. Accordingly, applicants respectfully request the Examiner to reconsider and withdraw this rejection.

The Examiner's attention is also draw to Claim 62 which does recite a practical application. For this additional reason, reconsideration and withdrawal of this rejection in relation to this claim is respectfully requested.

Examiner's response:

The applicant's arguments persuaded the Examiner to reconsider the previous position and the Examiner withdraws the 35 U.S.C. §101 rejection

9. In reference to the Applicant's argument:

REJECTION UNDER 35 U.S.C. § 102
Claims 43-57, 59-76 and 78-80 stand rejected under 35 U.S.C. §102(b) as being unpatentable over a dissertation by Oh entitled "Analog CMOS Implementation of Artificial Neural Networks for Temporal Signal Learning" (Oh). This rejection is respectfully traversed.

Applicant's invention is directed generally to a self-programmable chip. Of note, Claim 44 recites that each synaptic cell in an array of synaptic cells stores weights for the cell locally in a capacitor and locally in a digital memory. Independent claims 62 and 81 recite similar subject matter. In contrast, Oh teaches that the capacitor for storing a weight is located outside an array structure as described on page 126, lines 3-9 of the dissertation. For at least this reason, we feel that the pending claims are patentably distinct from the relied upon reference.

The Examiner also relies on page 116, lines 2-17 of the dissertation to reject the pending claims. However, the Examiner has misinterpreted the teachings of this portion of the reference. For instance, this section does not describe an array architecture as recited in the pending claims, but rather discusses the general/generic approach on how to possibly refresh the weights. It does not detail how the interface is manifested or how many weights for that matter. It does not discuss timing issues or organization. It describes the costly process of possibly reading the weight values via an externally interface(s), with an A/D, then storing the weights on an external digital form, then refreshing the weights by an interface circuitry and D/A. It does not concern itself with how long this would take, how may weights it can handle, how the signal internally in

the chip is routed or switched from one weight to the other. On the face of it, it simply refers to this potential approach, and then it discards it in favor of the approach it describes in the second paragraph (see Oh, p 116:11-17).

This approach of storing the weights off-chip has may known limitations, e.g.,: (1) expensive discrete (not integrated) components, (2) does not preserve the weight value due to signal transfers along "long" wires inside and outside the chip (losses), (3) increase of noise and low SNR, (4) complexity of interface wiring inside and outside the chip to route the weight signal values from a specific location of the weight array to a single external A/D and D/A interface circuitry, (5) a non self-contained processing solution that always requires the interface to the external computing platform (e.g., a PC). Oh, then states that this approach will be expensive and thus proceeds to the approach in the second paragraph of this section (Section 5.6.4, Oh, p116:11-17) whereby one uses a duplicate (master) neural network to exclusively focus on the learning process and a slave network that uses a copy of the learned weights to maintain the weights as long as learning is on going. For these additional reasons, we feel that the teachings of the Oh reference are deficient as applied to the pending claims. Accordingly, Applicants respectfully request the Examiner reconsider and withdraw these rejections.

Examiner's response:

Roenker is used to disclose each circuit contains a capacitor which is employed to 'modify the synaptic weight' for each neuron circuit. This further illustrated 'Each of the coupling capacitors can have different values, thus weighting their respective inputs as desired. In addition the D.C. bias across each diode can be individually set to adjust the weight or efficiency of a given size input pulse depositing charge on input integrating capacitor.' Roenker discloses the construction of a neural network by numerous 'neuron circuit' by the following. 'In this manner, the electronic neuron circuit with multiple inputs and outputs can be used to interconnect many such neuron circuits together, thus forming a neural network.' Office Action stands.

Examination Considerations

10. The claims and only the claims form the metes and bounds of the invention. "Office personnel are to give the claims their broadest reasonable interpretation in light of the supporting disclosure. *In re Morris*, 127 F.3d 1048, 1054-55, 44USPQ2d 1023, 1027-28 (Fed. Cir. 1997). Limitations appearing in the specification but not recited in the claim are not read into the claim. *In re Prater*, 415 F.2d, 1393, 1404-05, 162 USPQ 541, 550-551 (CCPA 1969)" (MPEP p 2100-8, c 2, l 45-48; p 2100-9, c 1, l 1-4). The Examiner has the full latitude to interpret each claim in the broadest reasonable sense. Examiner will reference prior art using terminology familiar to one of ordinary skill in the art. Such an approach is broad in concept and can be either explicit or implicit in meaning.

11. Examiner's Notes are provided to assist the applicant to better understand the nature of the prior art, application of such prior art and, as appropriate, to further indicate other prior art that maybe applied in other office actions. Such comments are entirely consistent with the intent and sprit of compact prosecution. However, and unless otherwise stated, the Examiner's Notes are not prior art but link to prior art that one of ordinary skill in the art would find inherently appropriate.

12. Examiner's Opinion: Paragraphs 10 and 11 apply. The Examiner has full latitude to interpret each claim in the broadest reasonable sense.

Conclusion

13. The prior art of record and not relied upon is considered pertinent to the applicant's disclosure.

-U. S. Patent 6205556: Watanabe

-U. S. Patent 6137886: Shoureshi

-U. S. Patent 5875439: Engel

-U. S. Patent 5744967: Sorensen

-U. S. Patent 5717834: Werblin

-U. S. Patent 5764858: Sheu

-U. S. Patent 5519811: Yoneda

-U. S. Patent 5485908: Wang

-U. S. Patent 5343555: Yayla

14. Claims 43-48, 51-67, 70-88 are rejected.

Correspondence Information

15. Any inquiry concerning this information or related to the subject disclosure should be directed to the Examiner Peter Coughlan, whose telephone number is (571) 272-5990. The Examiner can be reached on Monday through Friday from 7:15 a.m. to 3:45 p.m.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor David Vincent can be reached at (571) 272-3080. Any response to this office action should be mailed to:

Commissioner of Patents and Trademarks,

Washington, D. C. 20231;

Hand delivered to:

Receptionist,

Customer Service Window,

Randolph Building,

401 Dulany Street,

Alexandria, Virginia 22313,

(located on the first floor of the south side of the Randolph Building);

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(571) 272-3150 (for formal communications intended for entry.)

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Peter Coughlan

9/27/2007

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